Bitstream Compression with Partial Reconfiguration

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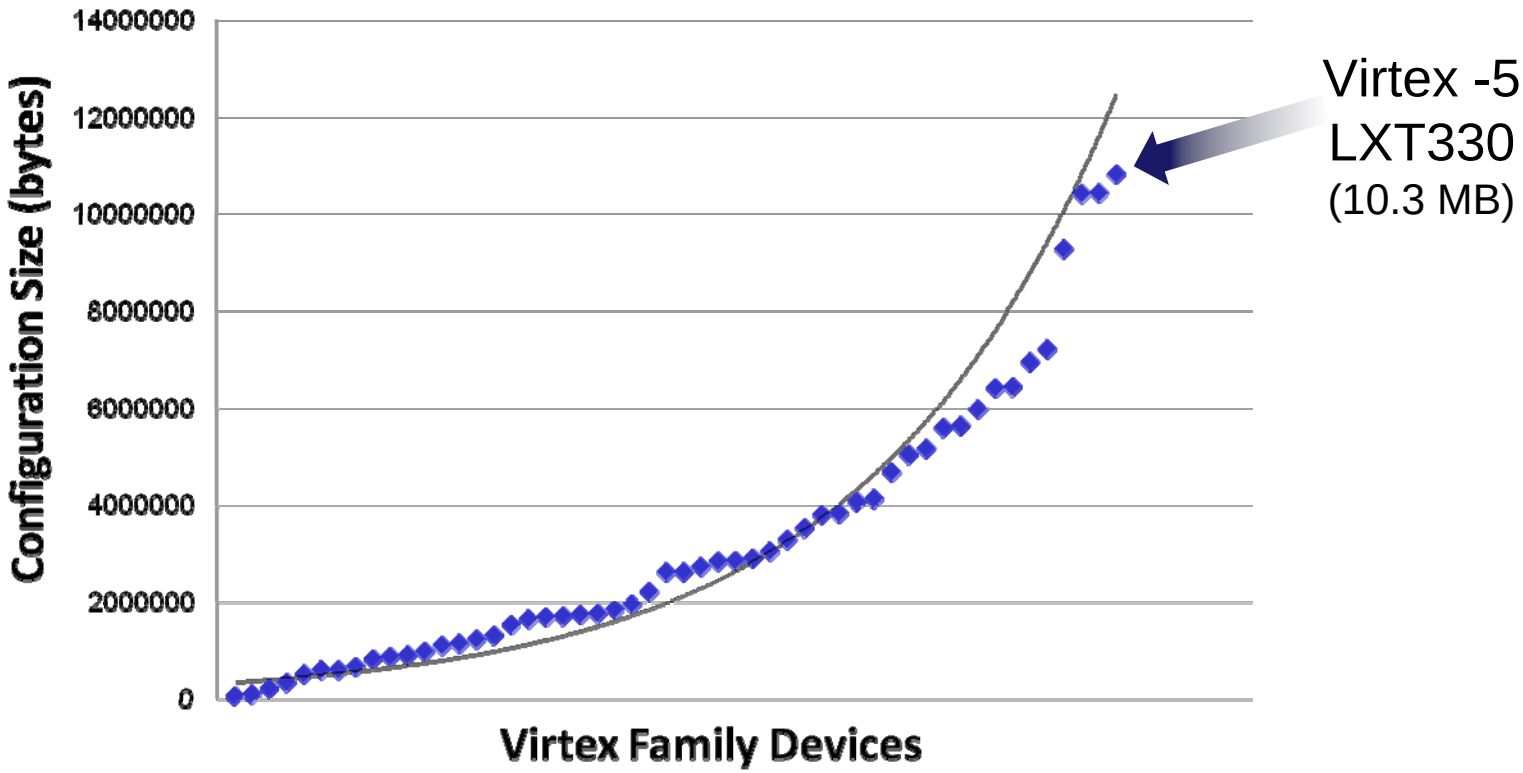
Increasing FPGA Configuration Size

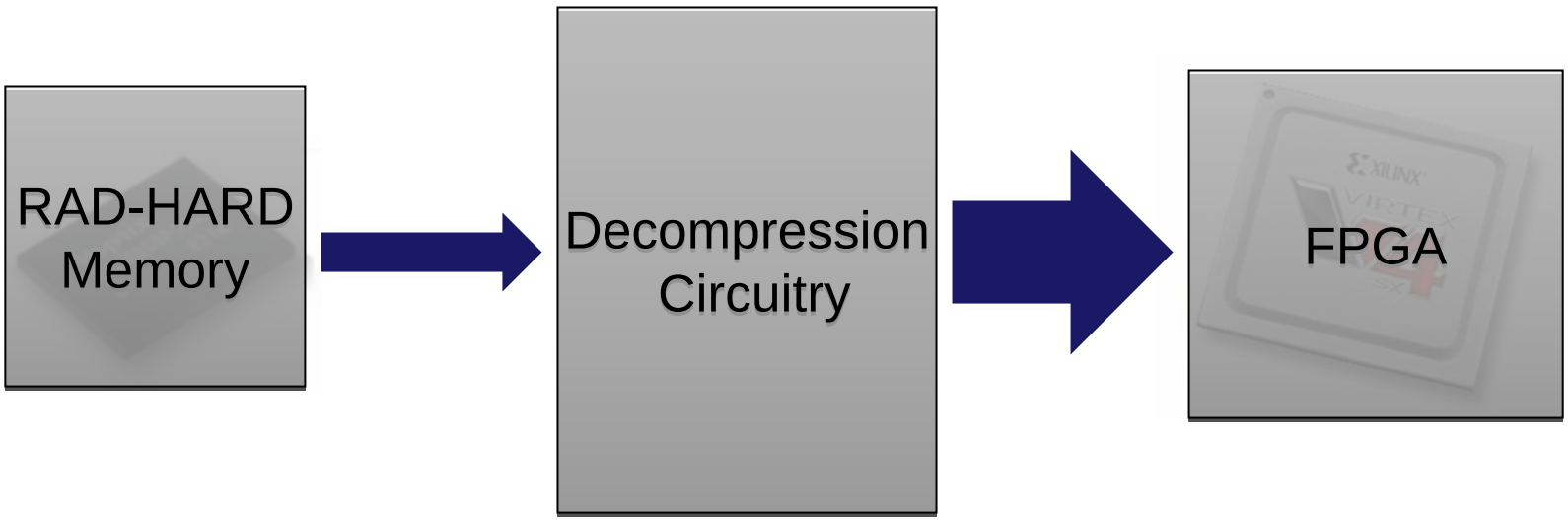
As FPGA density continues to increase, configuration bitstream sizes will continue to grow at the same rate



Bitstream Compression

Current Techniques

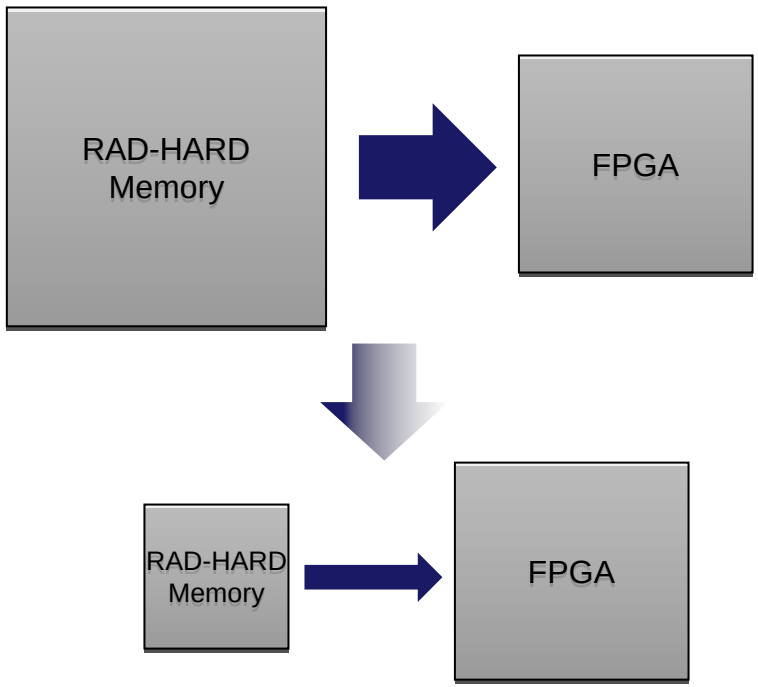
- Require on-board decompression
- Affected by size of the design



Techniques studied showed compression ratios of 1.32 to 7.00

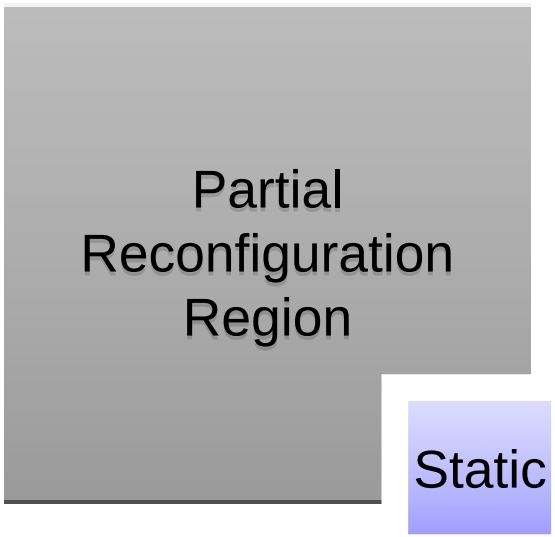
Goal

- Reduce the amount of configuration data that must be stored in non-volatile memory
- Eliminate the need for decompression circuitry



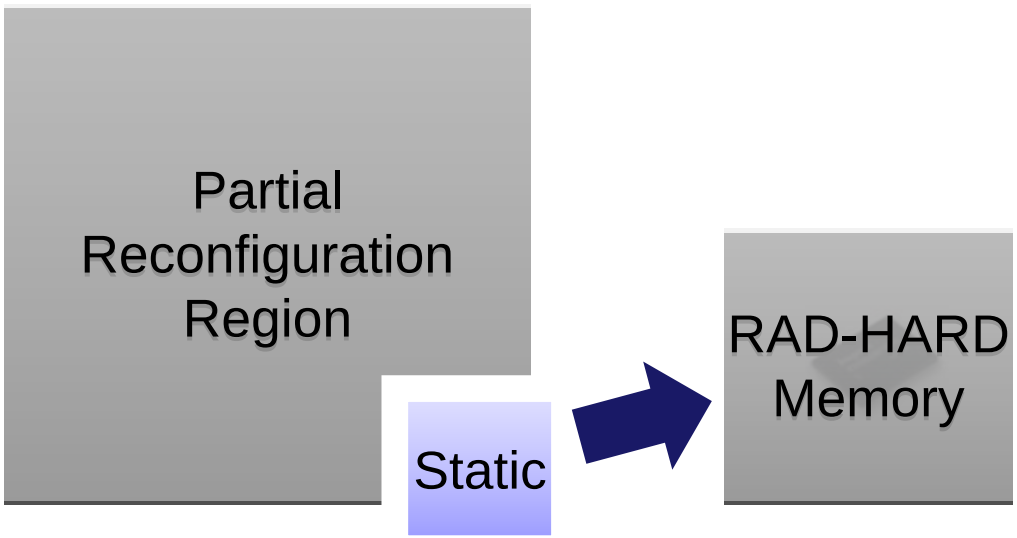
Key Points of Technique

1. Break up design into two components
   - Static region configured at initialization
   - Dynamic region configured after initialization through partial reconfiguration



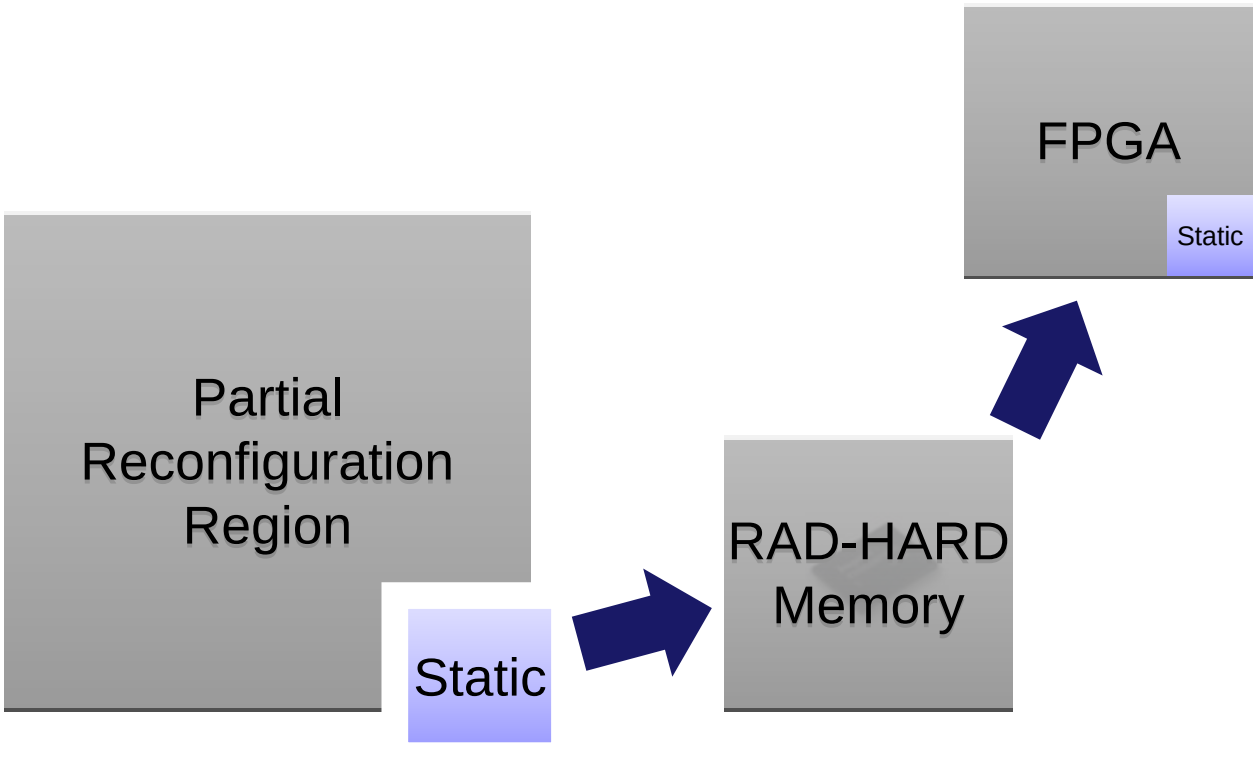
Key Points of Technique

2. Compress and store static design in radiation-hardened memory



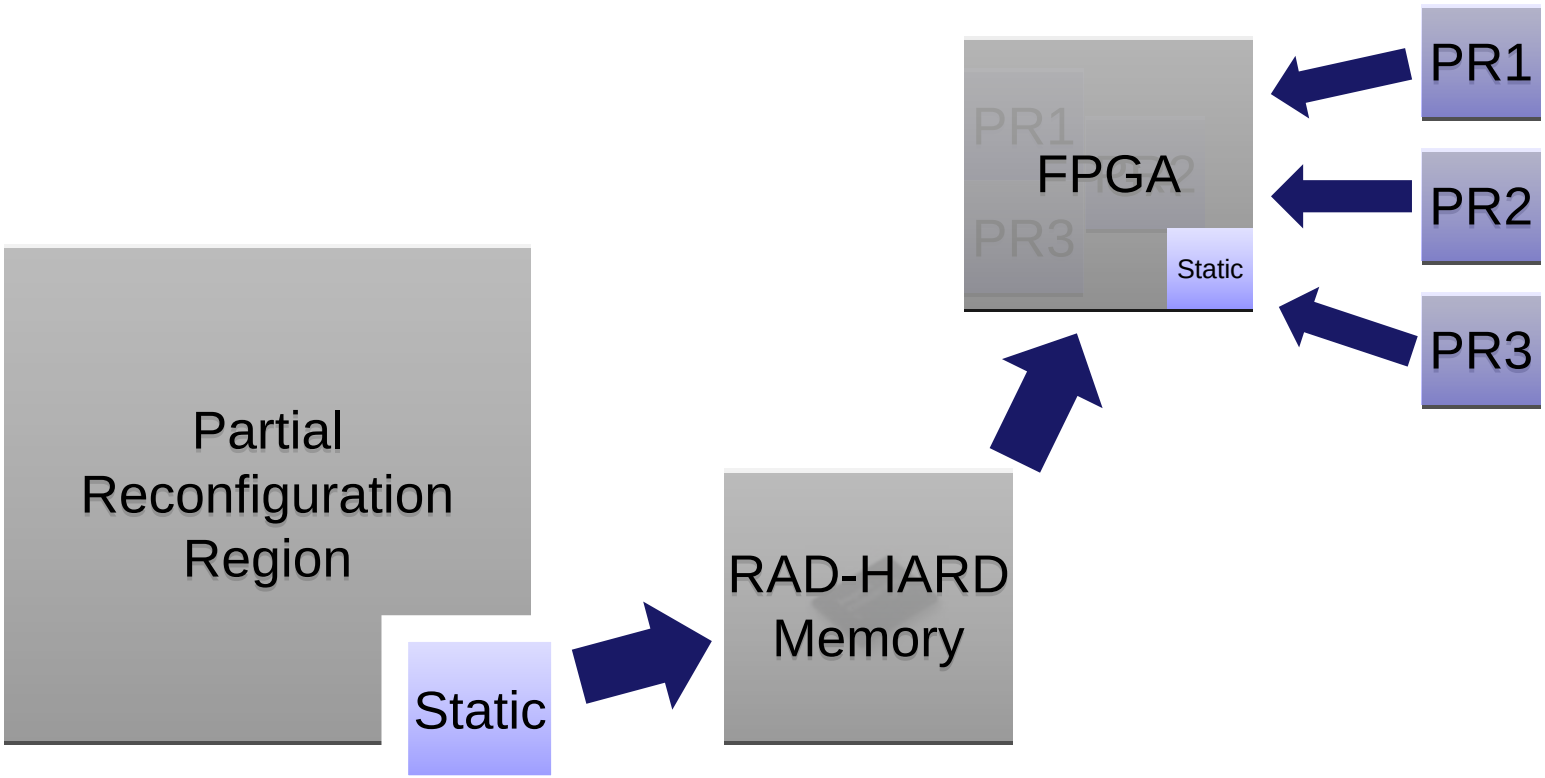
Key Points of Technique

3. Load static design from memory into FPGA

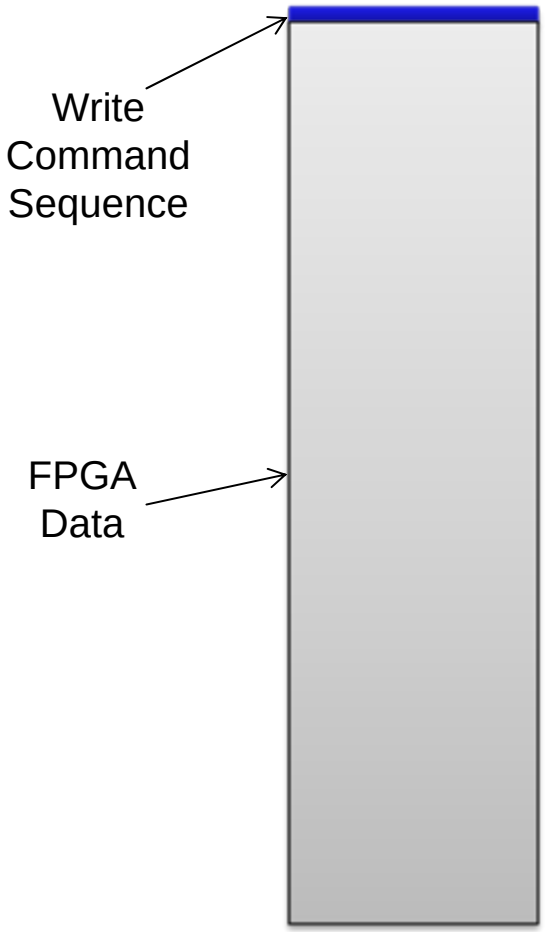


Key Points of Technique

4. Create larger, more complete designs by partially reconfiguring FPGA to add complex functionality

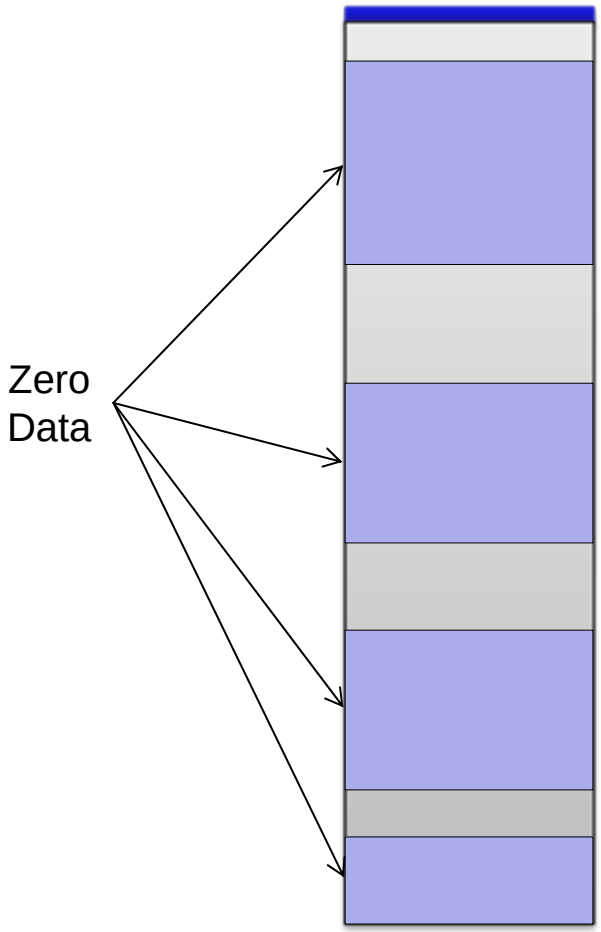


Bitstream Compression



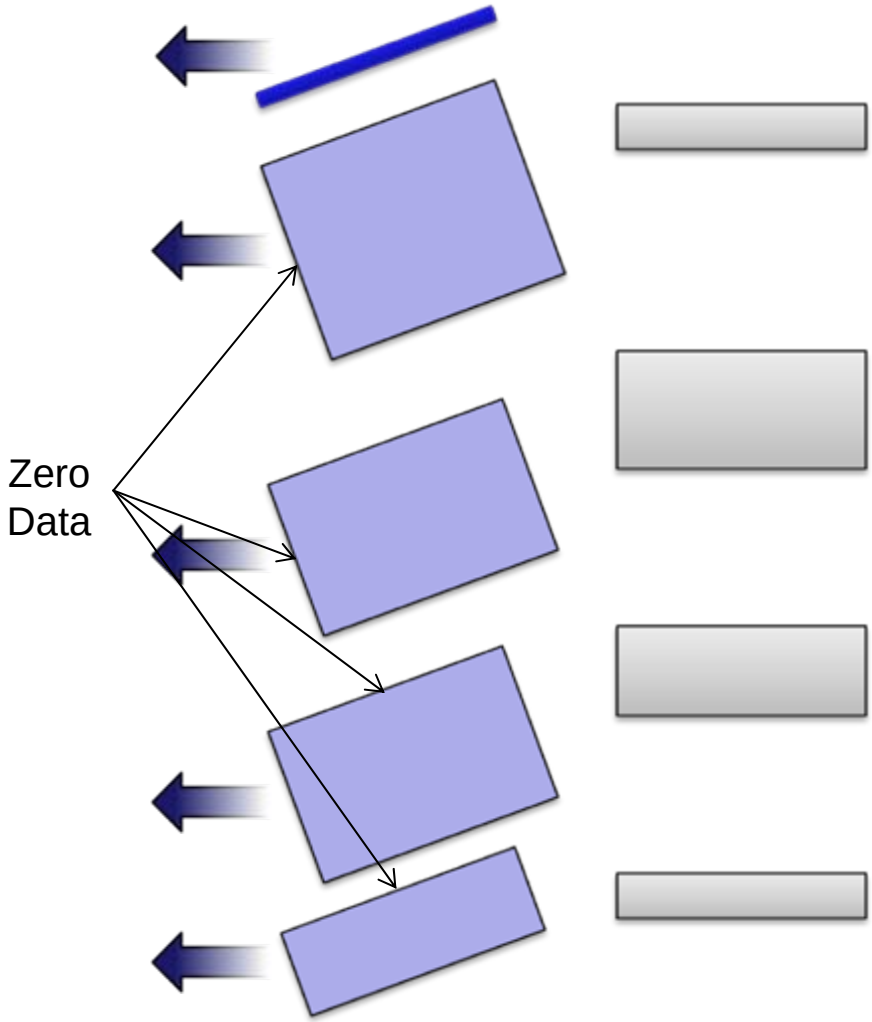
Full
Bitstream

Bitstream Compression



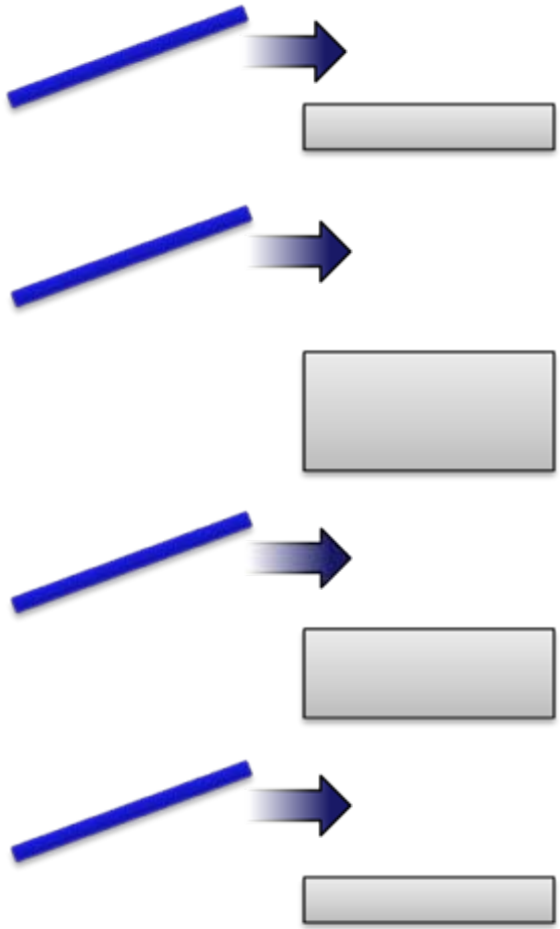
Identify unused logic

Bitstream Compression



Remove unused logic and old command sequence

Bitstream Compression

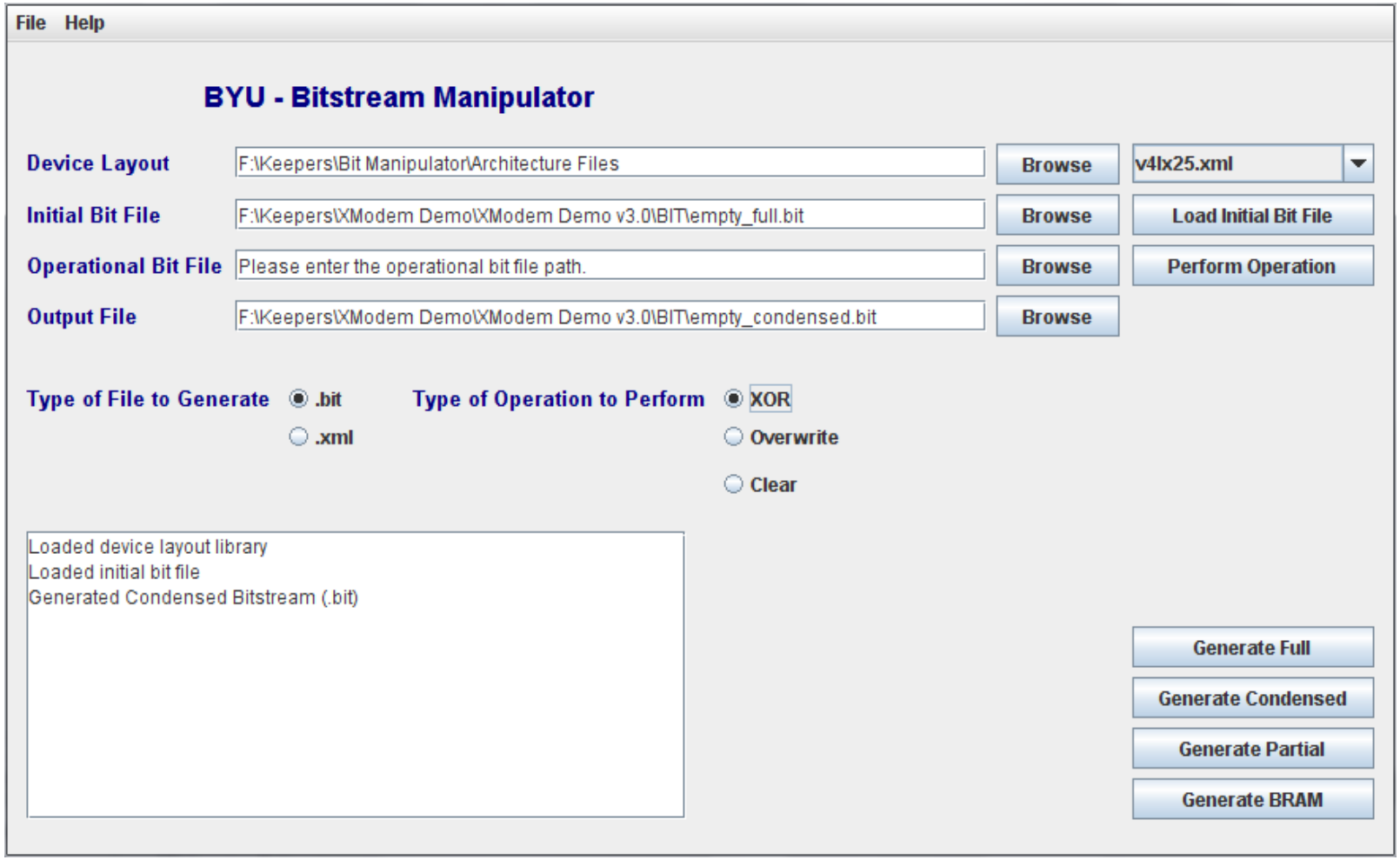


Add new write command sequences

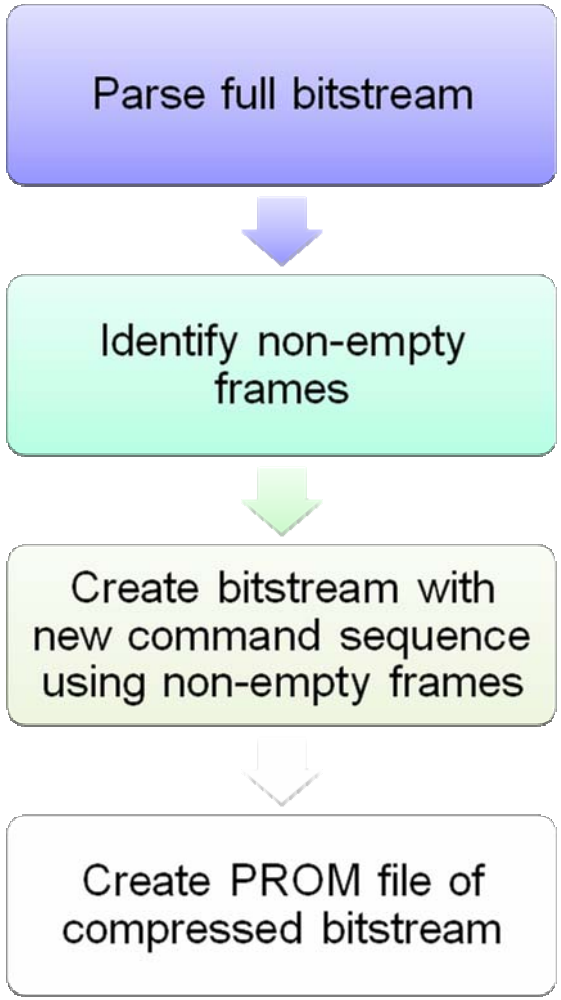
Bitstream Compression

Compressed
Bitstream

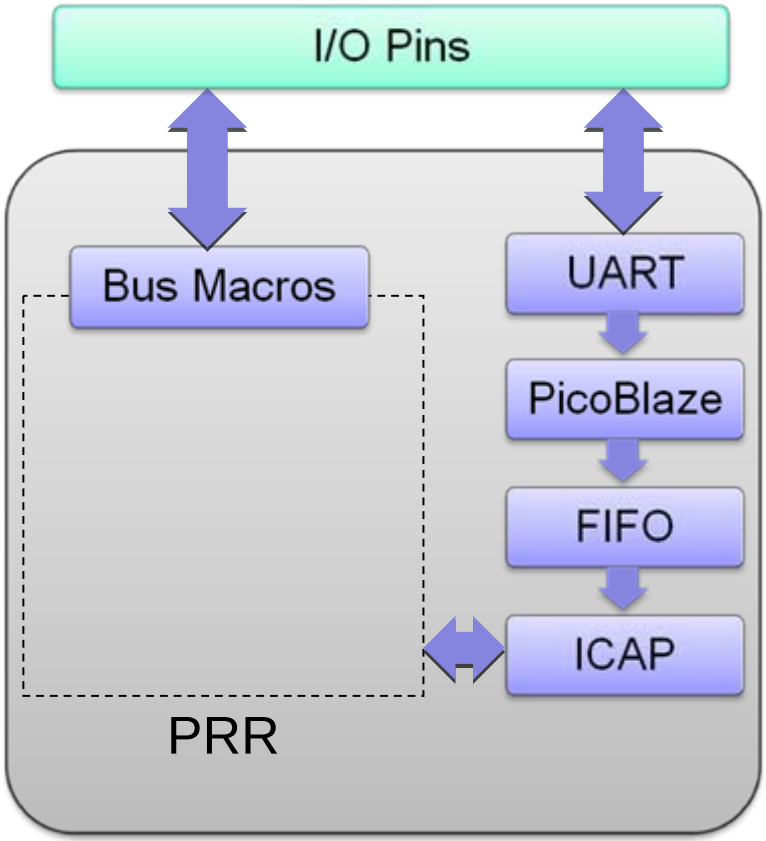
Bitstream Parser



Bitstream Compression Flow

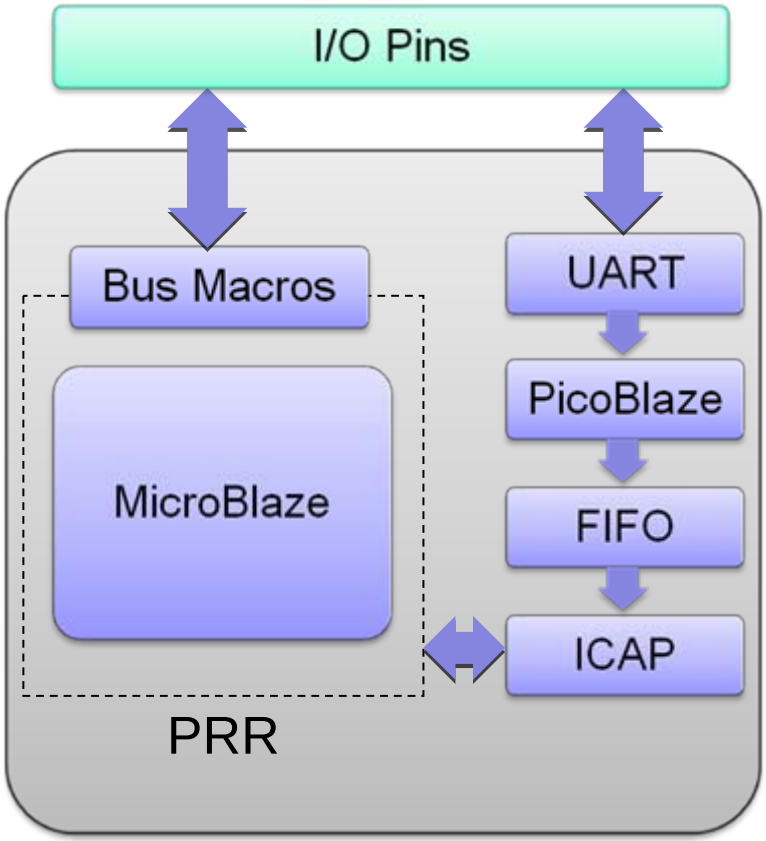


Demonstration Design



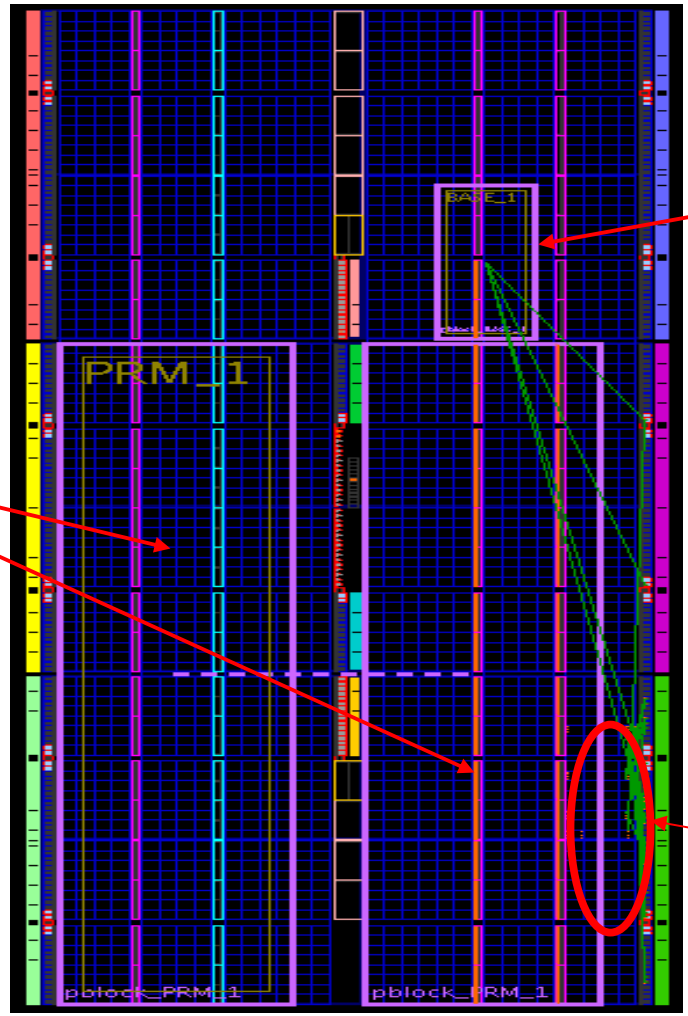
- Small initial design
  - 262/10752 Slices (2%)
- UART
  - Receives bitstream data
- PicoBlaze
  - Xmodem protocol
- FIFO
  - Stores received data until CRC can be performed
- ICAP
  - Performs partial reconfiguration
- Bus Macros
  - Restrict routing between the static and partial regions

Demonstration Design



- PR Modules
  - "Empty"
  - LED counter
  - MicroBlaze OLED display controller
  - ALU

Floorplanning and Placement

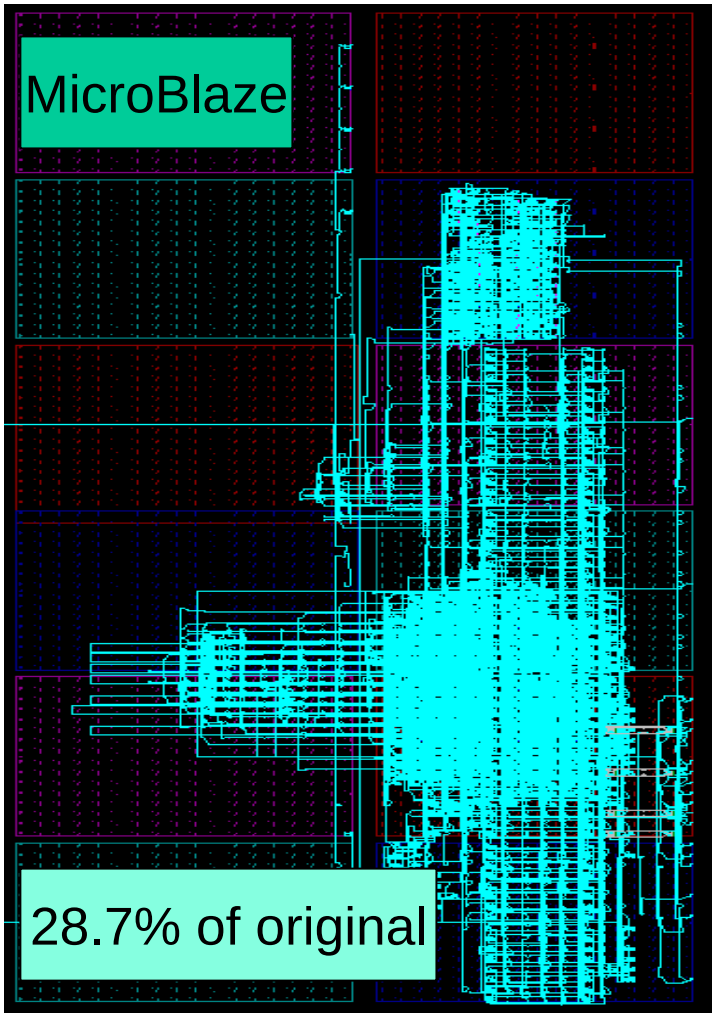


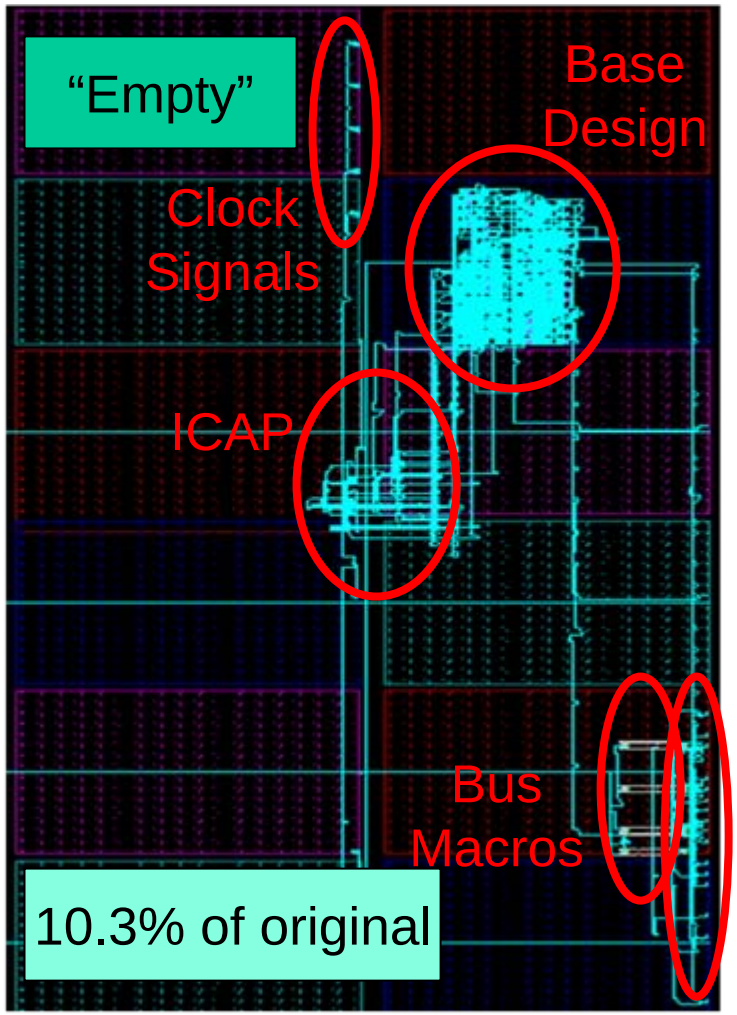
Base Module

Partial Module

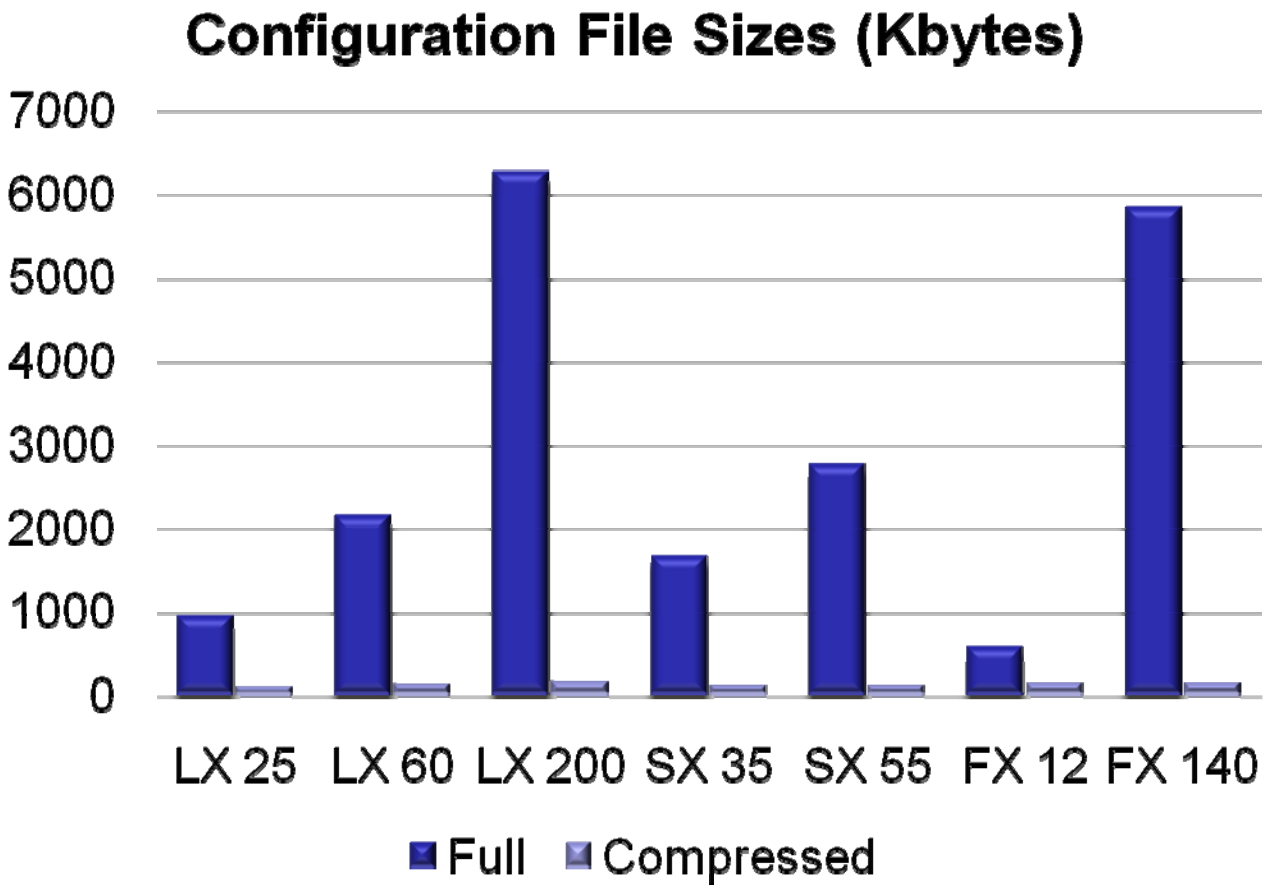
Bus Macros

MicroBlaze vs. “Empty”





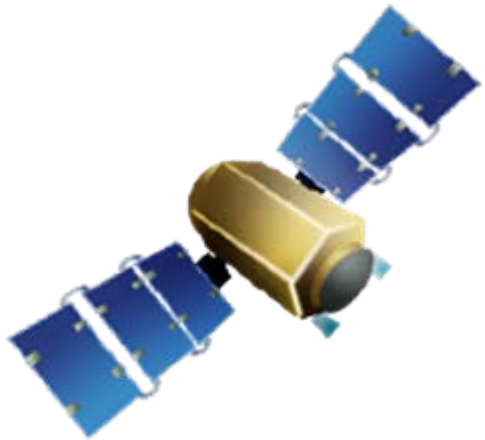
Virtex-4 Device Comparison



Device	%
LX 25	10.3%
LX 60	5.94%
LX 200	2.37%
SX 35	6.27%
SX 55	4.06%
FX 12	23.9%
FX 140	2.32%

Design Challenges

- Minimizing static logic
  - Placement considerations
  - Timing constraints
- Partial reconfiguration
  - PRR placement
  - Bus macros
- BRAM initialization
  - MicroBlaze support
  - Requires additional bitstream manipulation



Conclusion

- Built partial reconfiguration design with an initial communication circuit
- Compressed initial bitstream by 89.7% for a V4 LX25 using new technique
- Successfully configured partial region through the static design with a remotely received bitstream